A Low Power High Resolution Digital PWM with Process and Temperature Calibration for Digital Controlled DC-DC Converters

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Problem

- High resolution DPWM is needed
- Analog delay line cell is large in size
- Current high resolution DPWM with process and temperature dependence

Our Solution

- Digital differential delay line
- Process calibration
- Temperature calibration

Background

The basic concept of digital controlled DC-DC converter is illustrated in Figure 1, taking a Buck converter as an example. First, the voltage difference between \( V_{ib} \) (output feedback voltage) and \( V_{ref} \) (bandgap reference voltage) is quantized by a high resolution ADC, and a digital error signal \( e[n] \) is generated. Then the error signal \( e[n] \) is processed by a digital computing unit, which may include digital compensator, protection function and other control algorithm, and a duty ratio \( d[n] \) outputs to the DPWM. DPWM is actually a high resolution digital to time converter (DTC), which generates a pulse signal with its width modulated by the \( d[n] \) at fixed frequency. Finally, the pulse is used to control the on/off state of the power switches in order to regulate the output to a targeted value.

Diagram

- Temperature & Process Calibration
- Differential Tapped Delay Line Ring Oscillator
- DPWM Logic

Temperature Monitor

- Temperature-dependent Voltage Output

Process Monitor

- Process-dependent Output

Principle

A novel 12-bit DPWM with process and temperature calibration is proposed here as shown in Figure 2. Eight 1X cells and three 4X cells are connected into a ring oscillator frame. The low 3-bit (L0-L7) and middle 3-bit (M0-M7) are tapped out as denoted in Figure 2. The relationship of the low 6-bits signals is shown in Figure 3 (a), where \( T_d \) is the oscillation period of the delay line. The rising edge sequence is from L7 to L0 and M0 to M7. For the final DPWM pulse, the Low 3-bit determines the starting edge of the pulse and the high six bits [H6-H11] determines how many \( T_d \) is following, and the middle three bits determine the falling edge of the pulse. The total period is \( 2^6 \times T_d \) as illustrated in Figure 3 (b). A control voltage called \( V_C \) can adjust all the cells’ delay time. The control voltage is generated by the process and temperature calibration circuit, which works as follows. First, the process and temperature monitor circuits keep monitoring the process and temperature variations and output an analog output. The output is converted to digital code by two 2-bits flash ADC. Combining the information of process and temperature variations, an appropriate voltage is selected through a loop-up table.

Figure 1. Digital DC-DC converter

Figure 2. Proposed 12-bit hybrid DPWM with process and temperature calibration

Figure 3. Time chart of the proposed DPWM