An Area Effective 4Gb/s 3-Tap Decision Feedback Equalizer with a Novel Current-Integrating Summer

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Abstract

This work presents an area effective first-tap speculative Decision Feedback Equalizer (DFE) with a novel current-integrating summer in standard CMOS 180nm technology node. Unlike the conventional first-tap speculative DFE that two summers are required at two parallel paths for speculation, a single proposed summer with switched-capacitors added is able to drive two speculative paths together.

Introduction

In high-speed backplane (Fig. 1) transmission, the quality of transmitted data is highly reduced due to the limited bandwidth of transmission line. Inter-symbol interference (ISI), which is the dominant noise, makes one data bit broaden to greater than one unit interval (UI) as shown in Fig. 2. This long "tail" interferes with the succeeding bits and causes a high possibility of error in receiver’s data detecting process.

To overcome this difficulty, different methods for data equalization both in transmitter and receiver sides have been presented. Among these approaches, decision feedback equalizer (DFE) surpasses other equalizers because of its advantage that compensating ISI without amplifying noise. The diagram of DFE is shown in Fig. 3.

DFE stores and feeds back the previous decisions which have already been made by slicer. These regenerative data bits are multiplied with proper tap coefficients and then summed with the current signal. After correctly calibrating the summer coefficients, the post-cursor ISI is able to be fully eliminated.

To relax the first tap feedback timing constraint which is the most challenging part of DFE implementation, first-tap speculation method is commonly used by adding or subtracting the first tap coefficient in advance. However, with an extra parallel path, this method is implemented at the cost of additional hardware.

Proposed Design

The main part of the conventional summers used in two speculative paths is the same and redundant. Area inefficiency is obvious with the increasing of unspeculative tap number. Therefore, a new area effective DFE is presented in Fig. 6, in which a new current-integrating summer is proposed to separate the first speculative tap by using switched-capacitors. The summer schematic is shown in Fig. 7.

The proposed summer consists of two stages, which are current-integrating stage and switched-capacitor stage. Both of them work in reset phase and evaluation phase separately. In reset phase, the output of first stage are pulled up to supply voltage and the voltage at two sides of capacitor in second stage are prepared at the same time. In the following phase, the second and third tap coefficients are eliminated in the first stage and the first tap is then added on or subtracted from the current signal at the switched-capacitor stage.

Simulation Result

The proposed DFE consumes 16.8mW with 1.8V supply when equalizing 4Gb/s data passed over a channel with 28 dB loss at 2GHz (Fig. 8). Simulated eye diagram of 4Gb/s random data bit at the output of channel is presented in Fig. 9 (a), which shows nearly closed eyes. The opened eye diagram after the equalization of the proposed DFE is shown in Fig. 9 (b). The equalization performance of the proposed DFE with input signal in different amplitude is checked by shifting the clock signal from -0.3UI to 0.3UI. The pass/fail diagram is derived in Fig. 10, where the black and white area represent that the equalization is passed and failed, respectively.

Conclusion

In this work, a 3-tap half-rate DFE with first-tap speculation is designed using 180nm CMOS technology at 1.8V supply voltage. A novel area effective DFE is proposed where the four summers are reduced to two compared with the conventional design. By using switched-capacitors to separate the first speculative tap, two parallel paths for speculation can be driven by a single summer.

References

